CLAIMS

I claim:

1. A method for statically estimating a body voltage of one or more transistors which form digital partially depleted silicon-on-insulator circuit having a predetermined circuit topology comprising said one or more transistors and one or more nets connecting said transistors, comprising the steps of:

   a. obtaining one or more device models, each corresponding to one of said one or more transistors;

   b. abstracting each of said device models to generate one or more simplified electrical descriptions, each corresponding to one of said one or more transistors;

   c. checking said predetermined circuit topology to generate one or more sets of accessible states, each set corresponding to one of said one or more transistors and being indicative of whether under any allowable switching activity, the source, gate or drain could be high or low.

   d. determining one or more sets of reference state body voltage minima and reference state body voltage maxima, one for each of said one or more transistors, based on corresponding simplified electrical descriptions and corresponding sets of accessible states; and

   e. ascertaining one or more target state body voltage minima and target state body voltage maxima, one for each of said one or more transistors, based on said determined sets of reference state body voltage minima and reference state body voltage maxima.

2. The method of claim 1, wherein said device models are selected from the group consisting of an n channel Field Effect Transistor model and a p channel Field Effect Transistor model.

3. The method of claim 2, wherein said abstracting step comprises abstracting each of said n channel Field Effect Transistor models, if any, and each of said p channel Field Effect Transistor models, if any, to obtain one or more displacement voltages $d_{i,}$, and one or more steady-state reference voltages V_i^{Zero}, for each of said device models.

4. The method of claim 3, wherein said corresponding simplified electrical descriptions comprise said displacement voltages $d_{i,}$, and said determining step comprises determining said sets of reference state body voltage minima, and reference state body voltage maxima based on corresponding displacement voltages $d_{i,}$ and corresponding set of accessible states.

5. The method of claim 4, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, based on said determined reference state body voltage minima and maxima using full uncertainty estimation.

6. The method of claim 2, wherein said abstracting step comprises abstracting each of said n channel Field Effect Transistor models, if any, and each of said p channel Field Effect Transistor models, if any, to obtain one or more displacement voltages $d_{i,}$, steady-state reference voltages V_i^{Zero}, and forward bias reference voltages $V_i^{forward}$, for each of said device models.

7. The method of claim 6, wherein said corresponding simplified electrical descriptions comprise said displacement voltages $d_{i,}$, and said determining step comprises determining said sets of reference state body voltage minima, and reference state body voltage maxima based on corresponding displacement voltages $d_{i,}$ and corresponding set of accessible states.

8. The method of claim 7, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, based

on said determined reference state body voltage minima and maxima using accessibility analysis.

9. The method of claim 6, further comprising the step of performing active net tagging, after said checking step, on each of said one or more nets to determine whether any of said one or more nets will switch with regular frequency.

10. The method of claim 9, wherein said corresponding simplified electrical descriptions comprise said displacement voltages $d_{i,}$, and said determining step comprises determining said sets of reference state body voltage minima, and reference state body voltage maxima based on corresponding displacement voltages $d_{i,}$, and corresponding set of accessible states, and from said determination from said active net tagging.

11. The method of claim 10, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, based on said determined reference state body voltage minima and maxima using modified accessibility analysis.

12. The method of claim 6, wherein said abstracting step further comprises abstracting each of said n channel Field Effect Transistor models, if any, and each of said p channel Field Effect Transistor models, if any, to obtain one or more corresponding time constant characterizations, one for each of said device models.

13. The method of claim 12, further comprising the step of calculating signal probabilities and timing windows from said time constant characterizations, after said checking step, on each of said one or more nets, wherein said signal probabilities are determined by boolean analysis, and said timing windows are determined by timing analysis.

14. The method of claim 13, wherein said corresponding simplified electrical descriptions comprise said displacement voltages d_i, and said determining step comprises determining said sets of reference state body voltage minima, and reference state body voltage maxima based on corresponding displacement voltages d_i, corresponding sets of accessible states, and from said calculated signal probabilities and timing windows.

15. The method of claim 14, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, based on said determined reference state body voltage minima and maxima using probabilistic analysis.

16. A method for analyzing an electrical property of a digital partially depleted silicon-on-insulator circuit having a predetermined circuit topology comprising one or more transistors and one or more nets, comprising the steps of:

a. ascertaining a target state body voltage minimum and a target state body voltage minimum for each of said transistors in said circuit;

b. establishing an initial condition for said circuit by selecting either said target state body voltage minimum or said target state body voltage minimum for each of said transistors in said circuit;

c. applying a voltage to said circuit; and

d. measuring said electrical property of said circuit.

17. The method of claim 16, wherein said electrical property comprises a switching delay and said measuring step comprises measuring a delay between a switching input and a switching output as a constituent simulation for static timing analysis.

18. The method of claim 16, wherein said electrical property comprises noise and said measuring step comprises measuring noise on one or more nets in said circuit as a constituent simulation for static noise analysis.

19. The method of claim 16, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, using full uncertainty estimation.

20. The method of claim 16, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, using accessibility analysis.

21. The method of claim 16, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, using modified accessibility analysis.

22. The method of claim 16, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima, and one or more target state body voltage maxima, using probabilistic analysis.